IDW

Docket No.: 60188-725

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mitsuyasu OHTA, et al.	:	Confirmation Number: 3295
Serial No.: 10/751,525	:	Group Art Unit: 2133
Filed: January 06, 2004	:	Examiner:

For: FUNCTIONAL BLOCK FOR INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT, METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT, AND METHOD FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

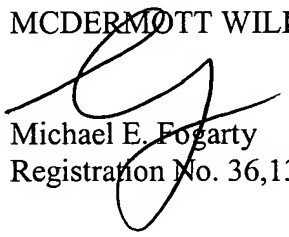
Each non-English language reference was first cited in a corresponding foreign application search report or office action and its relevance discussed therein. A copy of the

foreign search report or office action, together with an English language version thereof, is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
60188-725	**10/751,525**
APPLICANT: **Mitsuyasu OHTA, et al.**	
FILING DATE: **January 06, 2004**	GROUP: **2133**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	**5,258,985**	**11/02/1993**	**Spence et al.**	
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3 -Number 4 -Kind Code5 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
		EP 0472 818 A2	**03/04/1992**	**INTERNATIONAL BUSINESS MACHINES CORPORATION**		**X**	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		MO Chin Tsung., et al. " Self Diagnostic BIST Memory Design Scheme." IEEE, pp. 7-9, August 8, 1994	
		WUNDERLICH et al. " Bit-Flipping BIST." IEEE, pp. 337-343, November 10, 1996	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.